Digital Filter: Low-Pass Design & Implementation

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***Abstract*—This report discusses the design and implementation of low-pass filters, briefly visiting both their analog and digital domains. Basic passive filter types (RL and RC) are analyzed to identify their physical and electrical limitations, such as attenuation and loading effects.**

To overcome these, our group investigates active filter circuits using operational amplifiers. The study eventually lead us to the design of a fourth-order Butterworth low-pass filter, including the derivation of component values and digital filter coefficients for simulation in MATLAB and real-life lab implementation/testing.

***Index Terms*—Low-pass filter, Butterworth, Active filter, Analog-to-Digital Conversion, MATLAB simulation.**

I. Introduction

A low-pass filter is a fundamental circuit designed to pass low-frequency signals (below a cutoff frequency, ω_c) while attenuating frequencies above this limit.

In an ideal "brick wall" filter, the signal magnitude drops instantly to zero for all frequencies $\omega > \omega_c$. This behavior is characterized by the transfer function:

$$H(s) = \frac{\omega_c}{s + \omega_c}$$

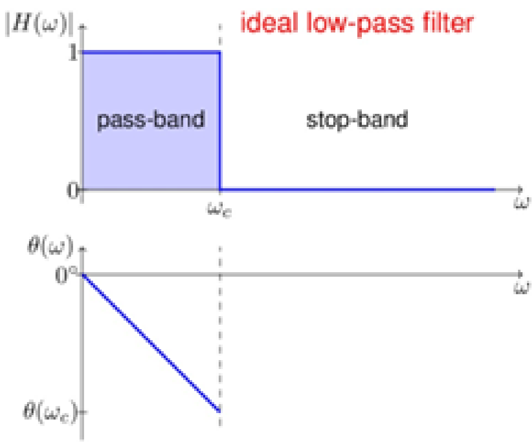

Fig. 1. Ideal low-pass filter response (Magnitude and Phase).

However, in real-life scenarios, filters must approximate this behavior with gradual transitions due to physical constraints. These filters are critical in applications such as audio processing for noise removal and data acquisition as anti-aliasing filters.

This report follows a structured analysis of filter types, moving from basic passive designs (RL/RC circuit) to advanced active Butterworth filters, and finally to digital signal processing simulations in MATLAB and real-life implementation.

II. Analog Signal Conditioning for Digital Systems

In digital system design, raw analog signals from sensors must be preprocessed before digitization to prevent aliasing (when the ADC undersamples a very fast sine wave signal) and ensure signal correctness.

This stage, called the Analog Front-End (AFE), uses passive and active filters to limit bandwidth and buffer signals for the ADC.

A. *Passive Low-Pass Filters (RC/RL Filters)*

The simplest form of signal conditioning uses passive components (Resistors, Capacitors, Inductors) to attenuate high-frequency noise that exceeds the Nyquist frequency of the digital system.

- **RC Filters:** Preferred for Digital PCBs due to low cost and compact footprint.
- **RL Filters:** Rarely used in compact digital hardware due to size, weight, price and parasitic capacitance of inductors.

We model these filters using Laplace transforms in the S-Domain to determine system stability and bandwidth.

The transfer function is $H(s) = \frac{\omega_c}{s+\omega_c}$.

The cutoff frequency ω_c (where power drops by -3dB) is defined as:

$$\omega_c = \frac{1}{RC} \quad \text{(for RC)}, \quad \omega_c = \frac{R}{L} \quad \text{(for RL)}$$

B. *Limitations of Passive Filters in Digital Hardware*

While passive filters are simple, they introduce significant issues when interfacing with modern ADCs.

1) Signal Attenuation: Passive filters generally have a gain ≤ 1. If the sensor signal is weak (e.g., millivolts), a passive filter cannot amplify it to fill the ADC's dynamic range, resulting in a loss of resolution (using fewer bits of the ADC). (See Appendix A).

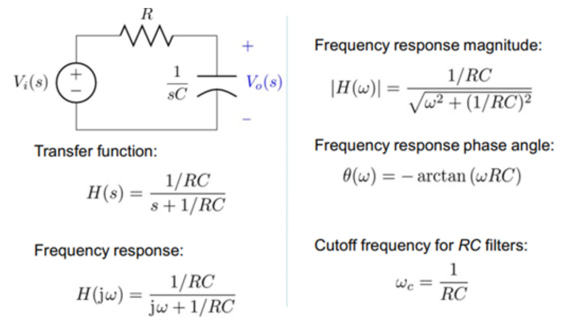

Fig. 2. RC Circuit & Transfer function Analysis.

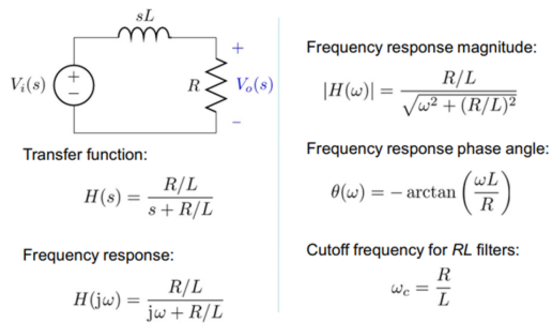

Fig. 3. RL Circuit & Transfer function Analysis.

2) Impedance Mismatch (Loading Effect): Digital ADCs often have specific input impedance requirements. Connecting a high-impedance passive filter directly to an ADC can distort the voltage reading ($V_{measured} \neq V_{signal}$), effectively shifting the calculated cutoff frequency. (See Appendix B).

C. The Active Solution: Op-Amp Buffers

To solve loading and gain issues, Operational Amplifiers (Op-Amps) are introduced between the sensor and the ADC.

- **Buffering:** Op-amps provide high input impedance (to not load the sensor) and low output impedance (to drive the ADC).
- **Gain:** They can amplify weak signals to maximize ADC resolution.
- **Limitation:** The transition from passband to stopband is not sharp enough for many applications. For a first-order filter, at $2\omega_c$ the magnitude is still 0.447 times the input (approx -7 dB), and at $10\omega_c$, it is only -20 dB. To achieve steeper roll-off, higher-order filters are required.

III. Advanced Design

A. Design A: Cascaded Identical Low-Pass Filters (Simple Approach)

A simple approach to achieve a 4th-order roll-off is cascading two identical 2nd-order filters.

1) Design Challenge: When identical filters are cascaded, attenuation adds up, shrinking the bandwidth. For a 4th-order cascade of identical stages, the cutoff frequency of each individual stage must be shifted to ensure the total system

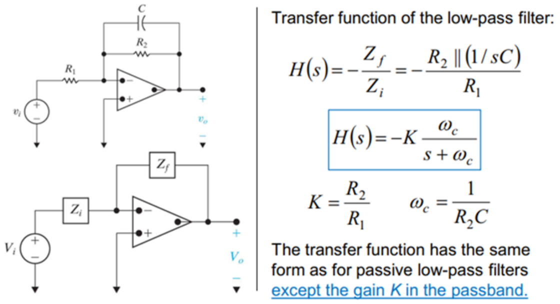

Fig. 4. Op-amp circuit & Transfer function Analysis.

has a -3dB point at 40 Hz. Using the derivation provided in Appendix C, the required cutoff frequency for the prototype filter is calculated as:

$$\omega_{c4} = \sqrt{\sqrt[4]{2} - 1} \approx 0.435 \text{ rad/s}$$

2) Component Selection: A standard capacitor value of $C = 1\,\mu\text{F}$ is selected for all stages to simplify things. Using the frequency scaling factor derived above ($k_f \approx 577.76$), the required resistor value is calculated as:

$$R = 1730.811\,\Omega$$

To achieve the total passband gain of 10, an inverting amplifier stage was added at the end with $R_f = 17.3\,\text{k}\Omega$ and $R_{\text{in}} = 1.73\,\text{k}\Omega$.

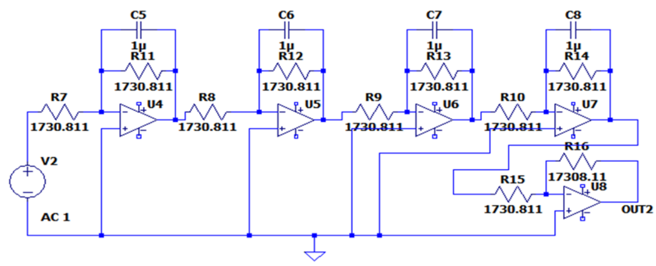

Fig. 5. Schematic of the Cascaded Identical Filter Design (Design A).

B. Design B: Fourth-Order Butterworth Filter (Optimal Approach)

To solve the "drooping" passband problem of Design A, we implemented a Butterworth filter. This design tunes the poles of each stage to different locations on the complex s-plane to achieve a maximally flat magnitude response. (Derivation in Appendix D).

1) Scaling Factors: Using the transfer function derived in Appendix A, we determined the following scaling factors to translate the mathematical model into real components:

- Frequency Scaling: $k_f = 2\pi(40) \approx 251.327$ rad/s.
- Magnitude Scaling: $k_m = 1000$ was selected to allow the use of standard $1\text{k}\Omega$ resistors, which are more readily available than the 1730Ω resistors used in Design A.

2) Final Component Values: $R = 1\text{k}\Omega$ for all filter stages. Capacitors are calculated based on these scaling factors as $C_1 = 10.385\mu\text{F}$, $C_2 = 1.512\mu\text{F}$, $C_3 = 4.297\mu\text{F}$, $C_4 = 3.676\mu\text{F}$. An inverting amplifier with $R_f = 10\text{k}\Omega$ and $R_{in} = 1\text{k}\Omega$ provides the required gain of 10.

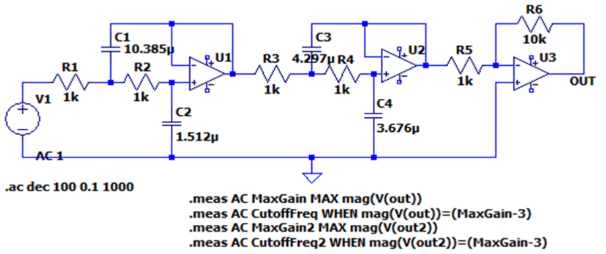

Fig. 6. Schematic of the 4th-Order Butterworth Design (Design B).

C. Simulation Comparison in LTSpice

Both designs were simulated in LTSpice to compare their frequency response. An AC sweep was performed from 100 mHz to 1 kHz.

Comparing Design A and B (Fig. 7):

- **Design B (Butterworth - Green):** Maintains a flat gain of approximately 20 dB almost exactly up to the cutoff frequency. This confirms our goal in Appendix D.
- **Design A (Cascaded - Blue):** Shows significant attenuation (droop) well before the cutoff frequency. Even though the -3 dB point is correct, the signal is attenuated by 1-2 dB inside the passband, which is undesirable for signal processing.

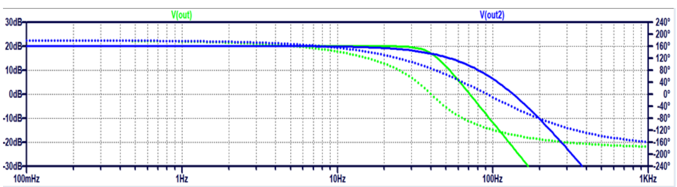

Fig. 7. Frequency response comparison. Green: Butterworth; Blue: Cascaded.

IV. Analog-to-Digital Conversion

The function of an Analog-to-Digital (A/D) converter is to transform a continuous-time analog signal into a discrete set of digital code words suitable for digital system processing. Simply put, A/D converter is the bridge between these two worlds. This conversion is a 3-stage process involving sampling, quantization, and coding.

A. First stage: Sampling

The main problem that need to be solved here is speed. An analog signal changes constantly. If we tried to measure it while it was moving, our reading would be blurred and invalid. A small interval of time freeze is needed so that the A/D converter can process the information before moving to the next sampling phase.

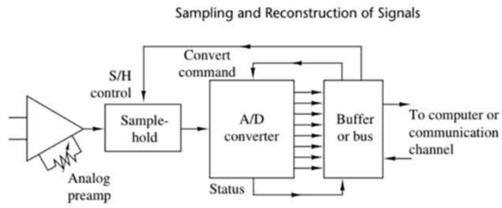

Fig. 8. Sampling and Reconstruction of Signals.

The solution to the mentioned problem is the Sample-and-Hold (S/H) circuit shown in the block diagram (Fig. 9), which is typically integrated directly into the A/D converter. The S/H circuit acts as the interface between the continuous analog input and the discrete digital conversion process.

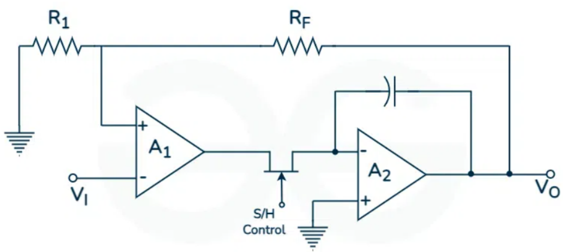

Fig. 9. Schematic of the Sample-and-Hold circuit

The circuit operates in two distinct modes (Fig. 10), "sample (S)" and "hold (H)":

- **Sample:** The transistor switch closes, the circuit tracks perfectly the instantaneous value of the analog input signal. Upon receiving a convert command, it switches to hold mode,
- **Hold:** The transistor switch opens, and the voltage is 'frozen' on the capacitor. This gives the ADC a stable, non-moving target to measure. It maintains the signal value constant while the A/D converter performs the conversion. This holding phase is critical because the conversion process requires a finite amount of time.

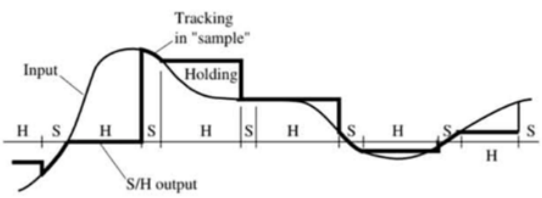

Fig. 10. Sample and Hold waveform graph

In the absence of an S/H circuit, if the input signal were to change by more than one-half of a quantization step during the conversion, the resulting digital representation would be invalid. Therefore, the S/H circuit is essential for high-resolution conversion of signals with large bandwidths.

There is one critical rule that must be followed:

$$F_s > 2F_0$$

This is the **Nyquist Condition**. It states that our sampling frequency (F_s) must be strictly greater than twice the maximum frequency of the input signal (F_0). If we sample any slower than this, aliasing will be introduced, where high-frequency signals distort and look like low-frequency noise. So, this condition is non-negotiable for an accurate conversion.

B. Second stage: Quantizing

Uniform Quantization

Quantization is the process of mapping a continuous range of input amplitudes into a finite set of discrete levels. Unlike sampling, which discretizes time, quantization discretizes amplitude. This is a nonlinear and non-invertible process where a continuous amplitude $x(n)$ at time $t = nT$ is mapped to a discrete amplitude x_k.

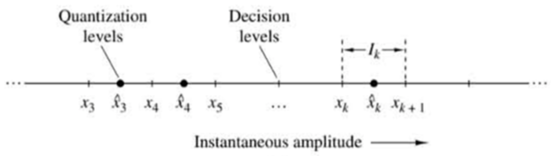

Fig. 11. Uniform Quantization levels.

The signal amplitude range is divided into L intervals, defined by decision levels $x_1, x_2, \ldots, x_{L+1}$. If the input signal $x(n)$ falls within a specific interval, it is assigned a corresponding quantization level $\hat{x}_k$.

In digital signal processing, it is standard practice to use uniform (or linear) quantizers. In a uniform quantizer, the range is divided into equal intervals, and the distance between adjacent quantization levels is constant. This distance is defined as the quantization step size or resolution, denoted by Δ:

$$\hat{x}_{k+1} - \hat{x}_k = \Delta$$

Midtread Quantization

A specific type of uniform quantizer, known as the midtread quantizer, is preferred in practical applications:

- If we look at the graph (Fig. 12), you will notice that the zero level sits right in the middle of a step.
- This is widely adopted because it allows us to represent silence or 0 volts perfectly, without oscillating between positive and negative values.

Quantization Error

Because the quantizer maps infinite input possibilities to a limited finite number of outputs, errors cannot be avoided. This is known as quantization error, $e_q(n)$. For a uniform quantizer, this error is bounded by half the step size:

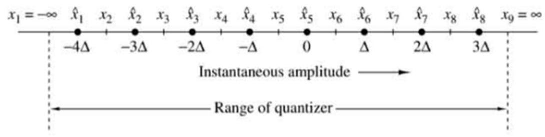

Fig. 12. Example of Midtread Quantizer

$$-\frac{\Delta}{2} < e_q(n) \leq \frac{\Delta}{2}$$

This inequality indicates that the instantaneous quantization error cannot exceed half of the quantization step. If the dynamic range of the input signal exceeds the range of the quantizer, clipping occurs, resulting in errors significantly larger than $\Delta/2$.

C. Third stage: Coding

The final stage of the A/D conversion is coding, where the quantized level $\hat{x}_k$ is assigned a unique binary sequence.

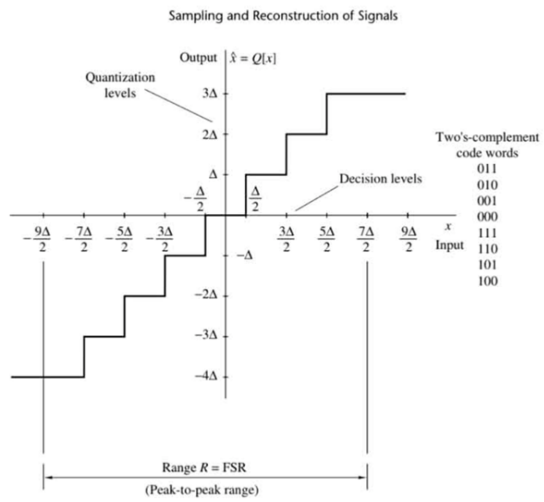

Fig. 13. Quantization characteristic and coding example of a midtread quantizer.

The number of bits available for this sequence determines the converter's resolution. With a word length of $b + 1$ bits, the system can represent 2^{b+1} distinct binary numbers. Consequently, the relationship between the full-scale range (R) of the quantizer and the step size (Δ) is given by:

$$\Delta = \frac{R}{2^{b+1}}$$

We typically use the Binary Value Equation shown at the bottom. For signal processing applications, the two's-complement format is most commonly used. It uses the first bit (b_0) as a sign bit, allowing our processor to easily handle both positive and negative voltages using standard arithmetic. In this formula, a $(b+1)$-bit binary fraction takes the form:

$$-b_0 \cdot 2^0 + b_1 \cdot 2^{-1} + b_2 \cdot 2^{-2} + \cdots + b_b \cdot 2^{-b}$$

Here, the conversion range is [-1, 1] volts. b_0 represents the most significant bit (MSB) and sign, while b_b represents the least significant bit (LSB).

V. Simulation and Lab Measurements

A. Experimental Setup

The physical validation was conducted using a breadboard implementation of the designed Butterworth circuit. The test signals were generated using an Agilent 33521A Waveform Generator, and the circuit's response was captured using a Rohde & Schwarz HMO2524 Digital Oscilloscope.

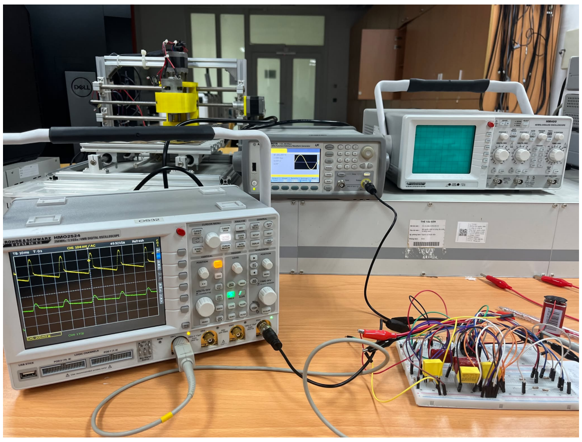

Fig. 14. Experimental Breadboard Setup.

B. MATLAB Simulation

Before physical testing, the filter behavior was simulated in MATLAB Simulink (Fig. 15).

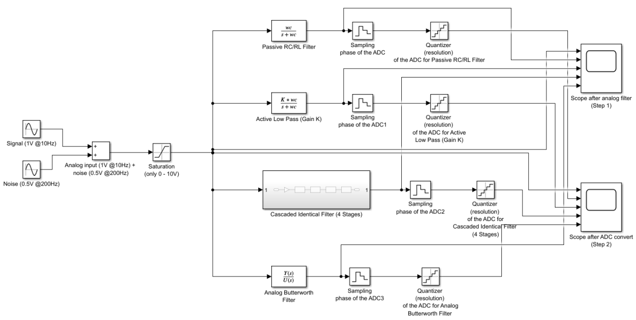

Fig. 15. MATLAB Simulink Setup.

We must processed a noisy signal through four different filter types before converting it to digital. The first Simulink stage compared the output signal of various filters to the input signal (Fig. 16):

Input signal and noise with saturation enabled (Yellow), Passive RC/RL (Blue), Active Low Pass (Red), Cascaded (Green), and the Analog Butterworth Filter (Purple).

- **Observation:** The Butterworth filter (purple) produces the smoothest output waveform, effectively reconstructing our ideal analog signal while removing the high-frequency "sawtooth" ripple seen in the passive and cascaded filter outputs.
- **Performance:** It demonstrates superior noise filtering compared to the Passive RC/RL filter (Blue), which still retains significant high-frequency distortion.

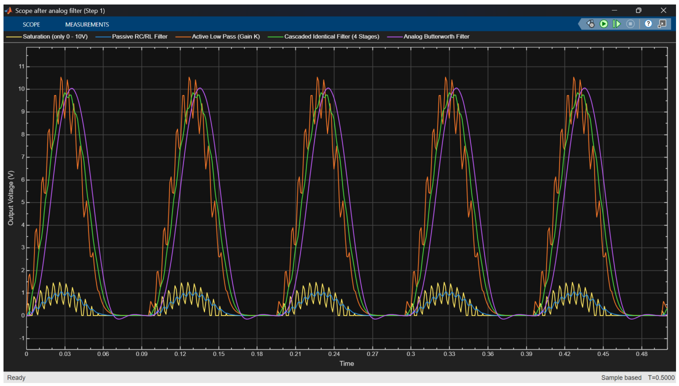

Fig. 16. MATLAB Simulink First Stage

For the second Simulink stage (Fig. 17), we used an 8-bit A/D converter with a saturation range of 0 to 10 volts. The saturation ensures there are no negative signals, as seen in the graph where the floor is at 0V. If we look at the graph, the results become very clear:

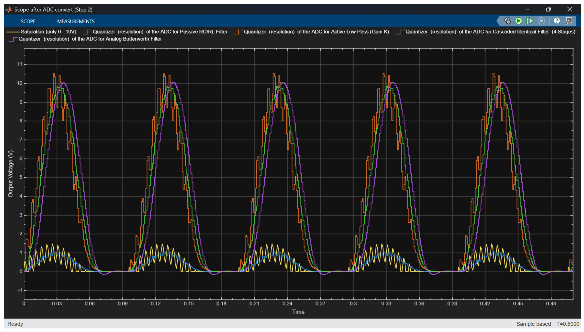

Fig. 17. MATLAB Simulink Second Stage

- **Analog Butterworth Filter:** It produces a smooth, monotonic staircase. This is our ideal signal output.
- **Other filters:** We can notice how the steps in the staircase are jagged and uneven. The filters failed to remove enough high-frequency noise, causing the converter to 'jitter' between values. These represent poor A/D conversions.

C. Hardware Measurements (Time Domain)

The laboratory measurements closely mirror the simulation results. The oscilloscope capture below (Fig. 18) displays the real-time response of the circuit to a noisy square-wave-like input.

- **Channel 1 (Yellow):** Input Signal. We pay attention to the sharp vertical transitions and "spikes," indicating high-frequency harmonic content and noise.

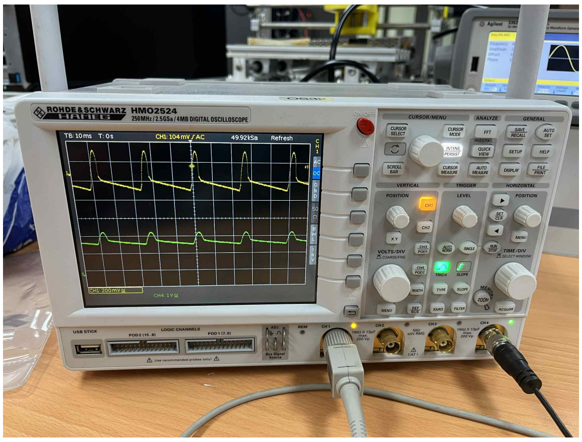

Fig. 18. Oscilloscope Capture: Input (Yellow) vs Output (Green).

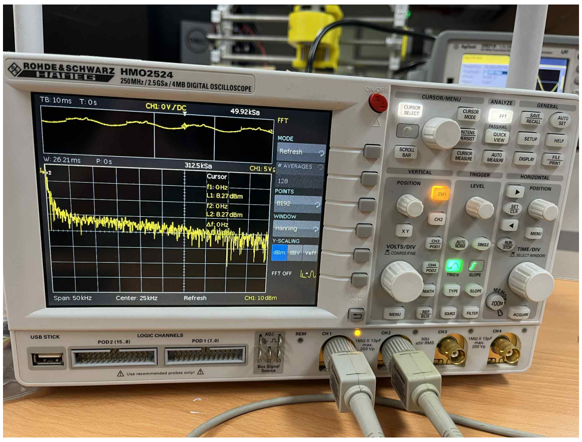

Fig. 19. FFT Spectral Analysis of the Filtered Signal.

- **Channel 2 (Green):** Output Signal (Filtered). The filter has smoothed the sharp edges into rounded peaks.
- **Comparison:** The shape of the Green trace here is nearly identical to the Purple trace in the MATLAB simulation (Fig. 16), confirming the theoretical model works in practice.

While the overall waveform shape matches the simulation, minor discrepancies in amplitude and phase delay are observable. These are attributed to non-ideal effects in the physical setup, including:

- **Component Tolerances:** Resistors and capacitors on the breadboard vary slightly from their rated values.
- **Parasitics:** The breadboard and jumper wires introduce stray capacitance and inductance.

D. Frequency Domain Analysis

To further validate the filter's performance, a Fast Fourier Transform (FFT) analysis was conducted on the oscilloscope (Fig. 19). This allows for the direct observation of the Cutoff Frequency (f_c) and the attenuation of harmonics. The oscilloscope was configured so that:

X-Axis displays Frequency (Span: 50 kHz, Center: 25 kHz).

Y-Axis displays Magnitude (dB).

- **Observation:** The spectrum shows a strong peak at the fundamental low frequency (left). As frequency increases, the magnitude drops significantly into the noise floor.
- **Cutoff Frequency:** The steep "roll-off" (the downward slope of the curve) confirms that frequencies above the designed cutoff are being actively attenuated. This explains why the sharp "corners" of the square wave (which consist of high-frequency harmonics) were removed in the time-domain graph.

To examine the cutoff behavior in detail, a zoomed-in capture was taken in Fig. 20 (Span: 2 kHz, Center: 40 Hz). As observed, with the center frequency locked at 40 Hz, the signal amplitude (dBm) drops significantly immediately beyond this point. This sharp decrease in magnitude confirms the effective attenuation of harmonics just above the fundamental frequency.

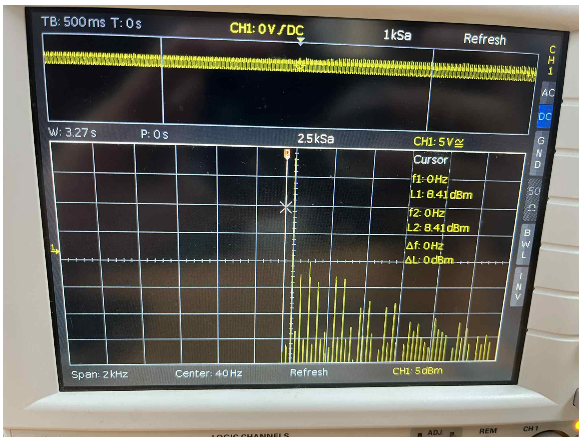

Fig. 20. Zoomed FFT Analysis showing amplitude drop after 40 Hz.

VI. Conclusion

This project successfully analyzed the theoretical foundations of low-pass filters. While passive RL and RC filters provide basic functionality, they are limited by loading effects and signal attenuation. Active op-amp filters solve these issues but require higher-order designs for sharper frequency drop-off.

We successfully designed a fourth-order Butterworth filter meeting the 40 Hz cutoff and gain requirements, providing both the analog component values and the digital coefficients necessary for implementation.

A thorough and necessary comparison between theoretical data from MATLAB simulations and lab measurements was made in order to highlight the limitations of practical components. This has effectively demonstrated how real-world constraints impact filtering performance relative to ideal theoretical models.

References

[1] J. W. Nilsson and S. A. Riedel, *Electric Circuits*, 11th ed. Pearson, 2019.

[2] J. G. Proakis and D. G. Manolakis, *Digital Signal Processing*, 4th ed. Prentice Hall, 2006.

Appendix A: Signal Attenuation Limitation of Passive RL/RC Filter

A.1 Passive RC Circuit Analysis

We first examine the behavior of a standard passive first-order RC low-pass filter.

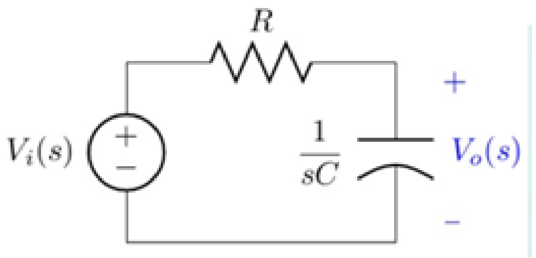

Fig. 21. Standard passive RC low-pass filter circuit.

The output voltage V_{out} is determined by the voltage divider rule formed by the resistor's impedance (Z_R) and the capacitor's impedance (Z_C):

$$V_{out} = V_{in} \times \frac{Z_C}{Z_R + Z_C}$$

Substituting the complex impedances $Z_R = R$ and $Z_C = \frac{1}{j\omega C}$:

$$H(j\omega) = \frac{V_{out}}{V_{in}} = \frac{\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}} = \frac{1}{1 + j\omega RC}$$

A.2 Magnitude Response Derivation

To find the magnitude of the transfer function (the gain), we calculate the absolute value of the complex ratio:

$$|H(j\omega)| = \left|\frac{V_{out}}{V_{in}}\right| = \frac{1}{\sqrt{1 + (\omega RC)^2}}$$

A.3 Proof of Gain Limitation (No Amplification)

A critical limitation of the passive RC filter is that the magnitude of the output signal can never exceed the magnitude of the input signal. This is proven mathematically by analyzing the denominator of the magnitude equation:

1) **Positivity:** The physical quantities angular frequency (ω), resistance (R), and capacitance (C) are all real, non-negative numbers.
2) **Squared Term:** Consequently, the term $(\omega RC)^2$ is always positive (or zero at DC, where $\omega = 0$).
3) **Denominator Value:** It follows that the denominator term is always greater than or equal to 1:

$$\sqrt{1 + (\omega RC)^2} \geq 1$$

4) **Resulting Gain:** Dividing 1 by a number greater than or equal to 1 results in a value less than or equal to 1:

$$|H(j\omega)| \leq 1$$

A.4 Conclusion

This proof confirms that $V_{out} \leq V_{in}$ for all frequencies. The passive filter can only attenuate the signal; it cannot amplify it. Since our design requirements specify a passband gain of 10 (20 dB), this limitation necessitates the use of active components (Op-Amps) and gain stages, as implemented in the main report design.

Appendix B: Loading Effect Limitations of Passive RL/RC Filter

Passive low-pass filters such as RC and RL filters suffer from a fundamental limitation known as the loading effect, which degrades filter performance when the output is connected to a finite load. Unlike active filters, passive filters' frequency response is strongly dependent on load impedance.

RC Low-Pass Filter with Load

For an ideal RC low-pass filter (output taken across the capacitor), the transfer function is:

$$H(j\omega) = \frac{V_{out}}{V_{in}} = \frac{1}{1 + j\omega RC}$$

with cutoff frequency:

$$f_c = \frac{1}{2\pi RC}$$

When a load resistance R_L is connected at the output, it appears in parallel with the capacitor. The effective resistance becomes:

$$R_{eq} = R \parallel R_L = \frac{RR_L}{R + R_L}$$

leading to a modified cutoff frequency:

$$f_c' = \frac{1}{2\pi R_{eq} C}$$

Since $R_{eq} < R$, the cutoff frequency increases ($f_c' > f_c$), causing a deviation from the designed response. Additionally, the low-frequency (passband) gain is reduced to:

$$|H(0)| = \frac{R_L}{R + R_L} < 1$$

indicating signal attenuation even in the passband.

Take the RL low-pass filter to be an illustration for how load effect can causes undesired changes to the frequency response of low-pass filter. For an RL low-pass filter (output taken across the resistor), the ideal cutoff frequency is:

$$f_c = \frac{R}{2\pi L}$$

With a load resistance R_L connected in parallel with R, the effective resistance becomes $R_{eq} = R \parallel R_L$, and the cutoff frequency changes to:

$$f_c' = \frac{R_{eq}}{2\pi L}$$

Because $R_{eq} < R$, the cutoff frequency decreases and the frequency response slope is altered.

Appendix C: Theoretical Basis and Circuit Derivations for Design A

C.1 Derivation of the Sallen-Key Low-Pass Transfer Function

Both the Cascaded (Design A) and Butterworth (Design B) filters utilize the Sallen-Key active topology. The general transfer function for a unity-gain Sallen-Key low-pass filter is derived from Kirchhoff's laws applied to the standard non-inverting op-amp configuration:

$$H(s) = \frac{V_o}{V_i} = \frac{\frac{1}{R^2C_1C_2}}{s^2 + \frac{2}{RC_1}s + \frac{1}{R^2C_1C_2}}$$

By normalizing the resistance values to R = 1Ω, the transfer function simplifies to:

$$H(s) = \frac{\frac{1}{C_1C_2}}{s^2 + \frac{2}{C_1}s + \frac{1}{C_1C_2}}$$

Matching this to the standard second-order polynomial form $H(s) = \frac{1}{s^2+b_1s+1}$, we can relate the coefficients to the component values:

$$b_1 = \frac{2}{C_1} \quad \text{and} \quad 1 = \frac{1}{C_1C_2}$$

These relationships allow us to calculate specific capacitor values (C_1, C_2) once the required polynomial coefficients are known from the Butterworth or Cascaded design tables.

C.2 Derivation of Cutoff Frequency Shift in Cascaded Filters

When n identical low-pass filters are cascaded, the total attenuation at any frequency increases, causing the overall bandwidth to shrink. We must derive the shifted cutoff frequency to correct for this effect.

Starting with the transfer function of a single normalized 1st-order prototype:

$$H_1(s) = \frac{1}{s+1}$$

The magnitude response of an n-stage cascade is the product of the individual magnitudes:

$$|H_{total}(j\omega)| = |H_1(j\omega)|^n = \left(\frac{1}{\sqrt{\omega^2+1}}\right)^n = \frac{1}{(\omega^2+1)^{n/2}}$$

To find the new cutoff frequency ω_{cn}, we set the total magnitude to -3dB (or $\frac{1}{\sqrt{2}}$):

$$\frac{1}{(\omega_{cn}^2+1)^{n/2}} = \frac{1}{\sqrt{2}}$$

Square both sides:

$$\frac{1}{(\omega_{cn}^2+1)^{n}} = \frac{1}{2}$$

Inverting and taking the n-th root:

$$\omega_{cn}^2 + 1 = 2^{1/n}$$

$$\omega_{cn}^2 = 2^{1/n} - 1$$

Solving for ω_{cn}:

$$\omega_{cn} = \sqrt{2^{1/n} - 1}$$

Application to Fourth-Order Design (n = 4):
Substituting n = 4 into the derived formula:

$$\omega_{c4} = \sqrt{\sqrt[4]{2} - 1} \approx \sqrt{1.1892 - 1} \approx \sqrt{0.1892} \approx 0.435 \text{ rad/s}$$

This factor indicates that a cascade of four identical filters will have a bandwidth that is only 43.5% of the bandwidth of a single stage.

C.3 Calculation of Adjusted Parameters for Design A (Cascaded)

To ensure the final cascaded system achieves the target cutoff frequency of $f_c = 40$Hz, we must pre-compensate the individual stages using the shift factor derived in Section C.2.

C.3.1. Frequency Scaling (k_f):: The target angular frequency is:

$$\omega_{target} = 2\pi(40) \approx 251.327 \text{ rad/s}$$

To compensate for the shrinkage factor (0.435), the individual stage cutoff frequency (k_f) must be increased:

$$k_f = \frac{\omega_{target}}{\omega_{c4}} = \frac{251.327}{0.435} \approx 577.764 \text{ rad/s}$$

C.3.2. Component Calculation:: For Design A, we selected a fixed capacitor value of C = 1 μF to minimize component complexity. Using the standard RC cutoff formula $\omega_c = \frac{1}{RC}$, we solve for the required resistance:

$$R = \frac{1}{k_f \times C} = \frac{1}{577.764 \times 10^{-6}} \approx 1730.811\,\Omega$$

Thus, Design A utilizes 1730.811 Ω resistors to achieve the corrected cutoff frequency.

Appendix D: Derivation of the 4th-Order Butterworth Transfer Function

D.1 Design Parameters

Based on the design requirements outlined in the Problem Description, the filter parameters are defined as:

- **Filter Order (n):** 4
- **Cutoff Frequency (f_c):** 40 Hz
- **Passband Gain:** 20 dB (Inverting configuration, $A_v = -10$)

First, the angular cutoff frequency (frequency scaling factor k_f) is calculated:

$$k_f = \omega_c = 2\pi f_c = 2\pi(40) \approx 251.327 \text{ rad/s.}$$

D.2 Normalized Butterworth Polynomial (n=4)

For a 4th-order Butterworth filter, the poles are located on the unit circle in the complex s-plane. The standard normalized denominator polynomial, $D_{norm}(s)$, is the product of two 2nd-order quadratic factors (obtained from standard Butterworth tables):

$$D_{norm}(s) = (s^2 + 0.765s + 1)(s^2 + 1.848s + 1)$$

Expanding this polynomial yields the 4th-order normalized denominator:

$$D_{norm}(s) = s^4 + 2.613s^3 + 3.414s^2 + 2.613s + 1$$

D.3 Frequency Scaling and Gain Adjustment

To transform the normalized filter (cutoff at 1 rad/s) to the target cutoff frequency ω_c, we apply the frequency scaling substitution $s \to \frac{s}{k_f}$. Additionally, the gain A_v is applied to the numerator:

$$H(s) = \frac{-10}{D_{norm}\left(\frac{s}{k_f}\right)}$$

$$H(s) = \frac{-10}{\left(\frac{s}{k_f}\right)^4 + 2.613\left(\frac{s}{k_f}\right)^3 + 3.414\left(\frac{s}{k_f}\right)^2 + 2.613\left(\frac{s}{k_f}\right) + 1}$$

Multiplying both the numerator and the denominator by k_f^4 to eliminate fractions:

$$H(s) = \frac{-10k_f^4}{s^4 + 2.613k_f s^3 + 3.414k_f^2 s^2 + 2.613k_f^3 s + k_f^4}$$

D.4 Final Coefficient Calculation

Substituting the scaling factor $k_f = 251.327$:

- **Numerator:** $-10 \cdot (251.327)^4 \approx -3.989 \times 10^{10}$
- s^3 **coeff:** $2.613 \times 251.327 \approx 656.7$
- s^2 **coeff:** $3.414 \times (251.327)^2 \approx 2.156 \times 10^5$
- s^1 **coeff:** $2.613 \times (251.327)^3 \approx 4.148 \times 10^7$
- s^0 **coeff:** $(251.327)^4 \approx 3.989 \times 10^9$

Final Transfer Function:

$$H(s) = \frac{-3.989 \times 10^{10}}{s^4 + 656.7s^3 + 2.156 \times 10^5 s^2 + 4.148 \times 10^7 s + 3.989 \times 10^9}$$